

In the United States Patent and Trademark Office

In re the application of
Hashimoto, et al.

TI-12592A.23

Serial No. 10/816,076

Art Unit: 2188

Filed: 3/31/2004

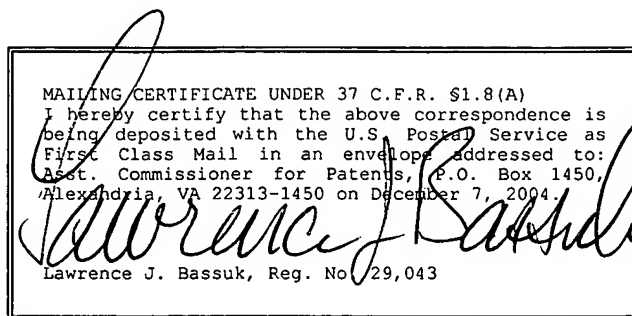
Examiner: J. Lane

Title: Synchronous DRAM System with Control Data

Information Disclosure Statement A, B, C, and D

December 7, 2004

Asst. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450



Dear Sir:

Applicants request consideration of the patents and other documents listed on enclosed forms PTO-1449.

Applicants combine four Information Disclosure Statements to bring art to the attention of the examiner. In previous applications, these four Information Disclosure Statements had been submitted separately. The separate statements identified the source of the listed references, as follows:

Information Disclosure Statement A had listed art from ancestor applications to this application, listed art from a later filed application for a synchronous DRAM and listed other patents owned by the assignee Texas Instruments Incorporated;

Information Disclosure Statement B had listed art cited in a search requested by Texas Instruments and conducted by the European Patent Office;

12/15/2004 JADD01 00000038 200668 10816076

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Information Disclosure Statement C had listed art cited in U. S. Patent 5,319,755 to Farmwald and assigned to RAMBUS, Inc.; and

Information Disclosure Statement D had listed art cited in U. S. Patent 4,789,960 to Willis, cited in the European search.

Each of the attached Forms 1449 identifies one of the above described Information Disclosure Statements as the source of the listed art.

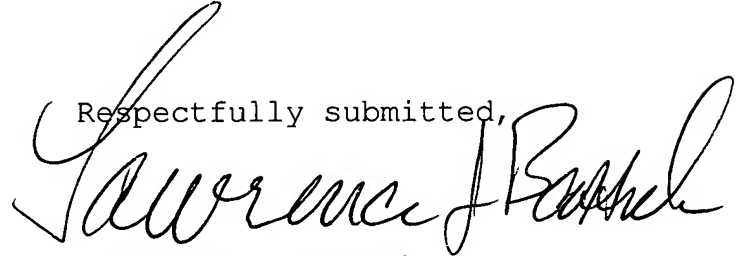
Under 37 CFR 1.98(d), no copy of the cited art is provided in this application. A copy of the cited art was previously cited and submitted to the Office in application Number 08/362,289, filed December 22, 1994. That application is relied upon for an earlier filing date under 35 U.S.C. 120.

Concise explanations of the listed patents and other documents that disclose a clock signal applied to or received by a memory part occur in Attachment A. Applicants' undersigned representative has looked at every listed reference and applicants believe that they have noted every patent or other document that discloses a clock signal applied to or received by a memory part; applicants cannot exclude however the possibility of unintentionally missing some such disclosure.

Under Rule 97(h), the filing of this information disclosure statement shall not be construed to be an admission that the information cited in this statement is, or is considered to be material to patentability as defined in Rule 56(b).

Please consider this statement as being filed under Rule 97(c), after the period specified in Rule 97(b), but before the mailing date of either a final action, or a notice of allowance. Under Rule 97(c), applicant submits the fee set forth in Rule 17(p). Please charge the fee under Rule 17(p) of \$130.00 to Deposit Account Number 20-0668 of Texas Instruments Incorporated. We enclose two copies of this sheet.

Respectfully submitted,



Lawrence J. Bassuk
Reg. No. 29,043
Attorney for Applicant

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, Texas 75265
(972) 917-5458

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INFORMATION DISCLOSURE STATEMENT A

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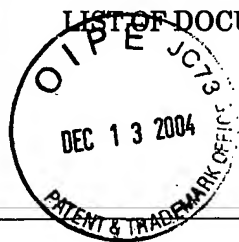
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| FORM PTO-1449 (REV. 7-80) | | U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | | ATTY. DOCKET NO. TI-12592A.23 | SERIAL NO. 10/816,076 |
| LIST OF DOCUMENTS CITED BY APPLICANT <i>(Use several sheets if necessary)</i> | | | | APPLICANT Hashimoto, et al. | |
| | | | | FILING DATE March 31, 2004 | GROUP 2188 |
| | | | | | |
| OTHER DOCUMENTS <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i> | | | | | |
| | | Bell Laboratories, Incorporated, <u>Transmission Systems for Communications</u> , 5th Edition, 1982, pp. 590-591. | | | |
| | | Cole, Bernard C., "Motorola's Radical SRAM Design Speeds Systems 40%, Electronics", July 23, 1987, pp. 66-68. | | | |
| | | Hashimoto, Masashi et al., "A 20-ns 256K X 4 FIFO Memory", IEEE Journal of Solid-State Circuits, Vol. 23, No. 2, April 1988, pp. 490-499. | | | |
| | | Hashimoto, Masashi et al., "A 20 ns 256K X 4 FIFO Memory", IEEE 1987 Custom Integrated Circuits Conference, May 4-7, 1987, pp. 315-318. | | | |
| | | Horowitz, Mark et al., "MIPS-X: A 20-MIPS Peak, 32-bit Microprocessor with On-Chip Cache", IEEE Journal of Solid-Circuits, Vol. SC-22, No. 5, October 1987, pp. 790-799. | | | |
| | | Lineback, J. Robert, "System Snags Shouldn't Slow the Boom in Fast Static RAMS", Electronics, July 23, 1987, pp. 60-62. | | | |
| | | Miyaguchi et al., "A Field Store System With Single 1Mbit Field Memory", IEEE Transactions on Consumer Electronics, Vol. 34, No. 3, August 1988, pp. 397-401. | | | |
| | | Morris, S. Brent et al., "Processes for Random and Sequential Accessing in Dynamic Memories", IEEE Transactions on Computers, Vol. C-28, No. 3, March 1979, pages 225-237. | | | |
| | | Motorola, "16Kx4 Bit Synchronous Statis RAM with Output Registers and Output Enable", Motorola Semiconductor Technical Data, MCM6293. | | | |
| | | Motorola, "16Kx4 Bit Synchronous Statis RAM with Output Registers and Output Enable", Motorola Semiconductor Technical Data, MCM6294. | | | |
| | | Nakagawa et al., "A 1 Mb Field Memory For TV Pictures", IEEE 1987 Custom Integrated circuits Conference, Pages 319-322. | | | |
| | | Ohara, Kazuhiro et al., "A Field Store System With Single 1Mbit Field Memory, ICCE Digest of Technical Papers", pages 70-71, June, 1988. | | | |
| | | Wada, R. et al., "A Color Television Receiver With Digital Frame Memory", 1966 IEEE Transactions on Consumer Electronics, Vol. 4, No. 3, pages 128-129. | | | |
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| | | | | | |
| EXAMINER | | | | DATE CONSIDERED | |
| +EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. | | | | | |

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2188

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(Use several sheets if necessary)



APPLICANT

Hashimoto, et al.

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U.S. PATENT DOCUMENTS

| +EXAMINER INITIAL | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE (IF APPROPRIATE) |
|----------------------|--------------------|---------|-------------------|-------|----------|---------------------------------|
| | 3,740,723 | 06/1973 | Beausoleil et al | 395 | 425 | |
| | 3,758,761 | 09/1973 | Henrion | 371 | 8.1 | |
| | 3,771,145 | 11/1973 | Wiener | 365 | 240 | |
| | 3,821,715 | 06/1974 | Hoff et al. | 340 | 173 | |
| | 3,882,470 | 05/1975 | Hunter | 364 | 200 | |
| | 3,924,241 | 12/1975 | Kronies | 395 | 425 | |
| | 3,969,706 | 07/1976 | Proebsting et al. | 365 | 189.02 | |
| | 3,972,028 | 07/1976 | Weber et al. | 395 | 425 | |
| | 3,975,714 | 08/1976 | Weber et al. | 395 | 800 | |
| | 3,983,537 | 09/1976 | Parsons et al. | 395 | 425 | |
| | 4,007,452 | 02/1977 | Hoff | 365 | 63 | |
| | 4,038,648 | 07/1977 | Chesley | 365 | 201 | |
| | 4,099,231 | 07/1978 | Kotok et al. | 395 | 425 | |
| | 4,191,996 | 03/1980 | Chesley | 395 | 425 | |
| | 4,205,373 | 05/1980 | Shah | 395 | 425 | |
| | 4,247,817 | 01/1981 | Heller | 307 | 354 | |
| | 4,249,247 | 02/1981 | Patel | 395 | 425 | |
| | 4,286,321 | 08/1981 | Baker et al. | 364 | 200 | |
| | 4,306,298 | 12/1981 | McElroy | 395 | 425 | |
| | 4,315,308 | 02/1982 | Jackson | 364 | 200 | |
| | 4,333,142 | 06/1982 | Chesley | 395 | 500 | |
| | 4,355,376 | 10/1982 | Gould | 365 | 200 | |
| | 4,373,183 | 02/1983 | Means et al. | 395 | 400 | |
| | 4,385,350 | 05/1983 | Hansen et al. | 365 | 229 | |
| | 4,443,864 | 04/1984 | McElroy | 395 | 325 | |
| | 4,449,207 | 05/1984 | Kung et al. | 365 | 189.02 | |
| | 4,468,738 | 08/1984 | Hansen et al. | 395 | 325 | |
| | 4,470,114 | 09/1984 | Gerhold | 395 | 325 | |
| | 4,481,625 | 11/1984 | Roberts et al. | 370 | 85 | |
| | 4,488,218 | 12/1984 | Grimes | 395 | 325 | |
| | 4,500,905 | 02/1985 | Shibata | 357 | 68 | |
| | 4,519,034 | 05/1985 | Smith et al. | 395 | 550 | |
| | 4,595,923 | 06/1986 | McFarland, Jr. | 340 | 825.5 | |

EXAMINER

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| OTHER DOCUMENTS <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i> | | | |
|---|--|---|--|
| | | Hawley, David, "Superfast Bus Supports Sophisticated Transactions," High Performance Systems, Sep. 1989. | |
| | | T. Yang, M. Horowitz, B. Wooley, "A 4-ns 4KX1-bit Two-Port BiCMOS SRAM," IEEE Journal of Solid-State Circuits, Vol. 23, No. 5, pp. 1030-1040 (Oct. 1988). | |
| | | "Burndy Connects Advertisement," Electronic Engineering Times, pp. T24-T25 (Feb. 24, 1986). | |
| | | A. Kahn, "What's the Best Way to Minimize Memory Traffic," High Performance Systems, pp. 59-67 (Sep. 1989). | |
| | | N. Margulis, "Single Chip RISC CPU Eases System Design." High Performance Systems, pp. 34-36, 40-41, 44 (Sep. 1989). | |
| | | R. Matick, "Comparison of Memory Chip Organizations vs. Reliability in Virtual Memories," FTCS 12th Annual International Symposium Fault-Tolerant Computing, IEEE Computer Society Fault-Tolerant Technical Committee, pp. 223-227 (Jun. 22, 1982). | |
| | | Agarwal et al., "Scaleable Director Schemes for Cache Consistency," 15th Intern. Sump. Comp. Architecture, pp. 280-289 (Jun. 1988). | |
| | | Agarwal et al., "An Analytical Cache Model," ACM Trans. on Computer Systems, Vol. 7 No.2, pp. 184-215 (May 1989). | |
| | | Davidson, "Electrical Design of a High Speed Computer Package", IBM J. Res. Develop., Vol. 26, No. 3, pp. 349-361 (1982). | |
| | | Hart, "Multiple Chips Speed CPU Subsystems", High-Performance Systems, pp. 26-55 (Sep. 1989). | |
| | | Beresford, "How to Tame High Speed Design", High-Performance Systems, pp. 78-83 (Sep. 1989). | |
| | | Carson, "Advance On-Focal Plane Signal Processing for Non-Planar Infared Mosaics," SPIE, Vol. 311, pp. 53-58 (1981). | |
| | | Horowitz et al., "MIPS-X: A 20-MIPS Peak 32-Bit Microprocessor with ON-Chip Cache," IEEE J. Solid State Circuits, Vol. SC-22, No. 5, pp. 790-799 (Oct. 1987). | |
| | | Kwon et al., "Memory Chip Organizations for Improved Reliability in Virtual Memories," IBM Technical Disclosure Bulletin, Vol. 25, No. 6, November 1982, pp. 2952-2957. | |
| | | Pease et al., "Physical Limits to the Useful Packaging Density of Electronic Systems," IBM J. Res. Develop. Vol. 32 No. 5, (Sep, 1988). | |
| | | Peterson, "System-Level Concerns Set Performance Gains," High-Performance Systems, pp. 71-77 (Sep. 1989). | |

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| EXAMINER | DATE CONSIDERED |
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GROUP

2188

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Wooley et al., "Active Substrate System Integration," Private Communication, Semiconductor Research Corporation, 4 pages (Mar. 15, 1988).

H. Schumacher, "CMOS Subnanosecond True-ECL Output Buffer," IEEE Journal of Solid-State Circuits, Vol. 25, No. 1, pp. 150-154 (Feb. 1990).

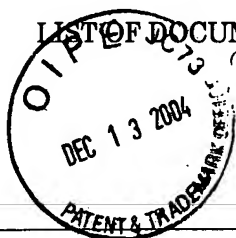
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| | | | | GROUP 2188 | |
| OTHER DOCUMENTS <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i> | | | | | |
| | | Kimura et al., "Power Reduction Techniques in Megabit DRAM's", IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 3, June 1968. | | | |
| | | Nogami et al., "1-Mbit Virtually Static RAM, IEEE Journal of Solid-State Circuits", Vol. SC-21, No. 5, October 1986. | | | |
| | | Ohta et al., "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 5, October 1986. | | | |
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